IN THE CLAIMS:

1. (Original) Automatic test equipment for testing a plurality of devices-under-test, each of the devices-under-test having a predetermined number of input/output contact points for receiving and outputting signals, said automatic test equipment including:

a plurality of channel modules, each of the channel modules having a plurality of channels, each channel corresponding to one of the contact points; and

calibrating 226 programmable delay circuitry coupled to each channel module, the programmable delay circuitry including a deskew circuit shared by more than one of the channels of the coupled channel module. + logic.

cl 26 at 29 delay lock loop

2. (Original) Automatic test equipment according to claim 1 wherein:

each channel module comprises an integrated circuit formed with more than one channel.

3. (Original) A method of calibrating channels of a parallel tester having calibration circuitry shared with tester channels, the method including the steps of:

determining the level of accuracy required from the calibration circuitry to calibrate the channels;

collecting deskew data for the channels;

optimizing the collected deskew data; and

storing the deskew data.

4. (Original) A method of calibrating channels of a parallel tester according to claim 3 wherein said optimizing step includes:

averaging the deskew data from more than one channel.

5. (Original) A method of calibrating channels of a parallel tester according to claim 3 wherein said optimizing step includes:

averaging the deskew data from all of the channels in parallel.

6. (Original) A method of calibrating channels of a parallel tester according to claim 3 wherein said optimizing step includes:

utilizing the individual deskew data for each channel.

7. (Currently Amended) A method of calibrating semiconductor tester channels for subsequently testing a plurality of ~~DUTs~~devices-under-test, the tester channels being formed into modules, the channels of each module coupled to pin locations for different ~~DUT~~ device-under-test locations, each module of channels having inputs coupled to shared calibration circuitry, the method including the steps of:

selecting a set of ~~DUT~~ device-under-test locations;

identifying each tester channel from each module coupled to the selected ~~DUT~~ device-under-test locations;

collecting deskew data for each of the identified channels with the shared deskew circuitry;

optimizing the collected deskew data;

storing the optimized deskew data for use during device testing; and

continuing the selecting, identifying, collecting, optimizing and storing steps until all of the tester channels are calibrated.

8. (Original) A method of calibrating semiconductor tester channels according to claim 7 wherein:

the optimizing step includes averaging the collected deskew data for groups of channels.

9. (Original) A method of calibrating semiconductor tester channels according to claim 7 wherein:

the optimizing step includes using the collected deskew data as the calibration data for each channel.

10. (Currently Amended) A method of testing a plurality of ~~DUTs~~ devices-under-test with a semiconductor tester, the tester including a plurality of channels formed into modules, the channels of each module coupled to pins of different ~~DUTs~~devices-under-test, each module of channels having inputs coupled to a shared programmable delay circuit, the method including the steps of:

selecting a group of ~~DUTs~~ devices-under-test to test;

identifying the channels from each module coupled to each pin of the selected ~~DUTs~~devices-under-test;

loading optimized calibration data for the identified channels into the programmable delay circuit;

testing the selected ~~DUTs~~devices-under-test; and

continuing the selecting, identifying, loading and testing steps until all of the ~~DUTs~~ devices-under-test are tested.

11. (New) Automatic test equipment for testing a plurality of devices-under-test, the automatic test equipment comprising:

a plurality of channels; and

a plurality of deskew circuits, the plurality of deskew circuits numbering less than the plurality of channels, the deskew circuits operative according to user-programmed steps comprising

in a high-accuracy mode

assigning each deskew circuit to an individual channel to provide a specified delay for each channel,

coupling the channels having assigned deskew circuits to the device-under-test,

testing the coupled devices-under-test, and

performing the coupling and testing steps until all of the devices-under-test are tested; and

in a low-accuracy mode

assigning each deskew circuit to a group of channels to provide an averaged delay for each channel,

coupling the channels to the devices-under-test, and

simultaneously testing all of the devices-under-test.

IN THE SPECIFICATION:

Page 4, lines 9 and 10:

A2 FIGs. 4a and 4b ~~is~~ are ~~a~~ flowcharts illustrating steps according to ~~another~~ other forms of the present invention; and

Page 5, lines 15 - 23:

A3 With particular reference to Figure 3, the calibration circuitry 40, according to one form of the invention, includes programmable delay circuitry 41 comprising a plurality of deskew circuits 42 connected to respective channel modules 46 (in phantom). Each channel module preferably comprises a plurality of driver/comparator channels 48 for straightforward implementation on an application-specific-integrated-circuit (ASIC). The net effect of this architecture results in the deskew circuits being shared by the channels of each module. Moreover, the channels of each module are preferably routed to different pin locations (1, 2, 3, and 4 of each DUT 24) to enable high accuracy calibration and testing as more fully described below.

Page 5, lines 24 - 30:

A4 Referring now to Figure 4a, the calibration method according to another form of the invention takes advantage of the shared deskew architecture described above by first determining the required level of accuracy, at step 100. If the accuracy requirements are moderate, then all of the channels of each channel module 46 are identified and activated, at step 102, to collect deskew data, at step 104, by skew detectors (not shown). Data collection may be effected by, for example, time-domain-reflectometry (TDR) procedures or any acceptable timing measurement method.

Page 5, lines 31 - 35:

A5 Once the data is collected, at step 104, the calibration software then optimizes the data for each module, at step 106, by determining the maximum range of skews between the channels, and finding an average compensating delay that provides the required test accuracy for each channel. The optimized data is then stored in a memory, at step 108, to be reloaded to each deskew circuit (programmable delay circuit) prior to device testing.

~~Page 6, lines 1 - 8:~~

A6 With ~~continuing~~ reference now to Figure 4b, high accuracy applications employ a similar calibration scheme to the moderate accuracy approach. The required level of accuracy is first determined (here, high) at step ~~100~~110, followed by collecting deskew data for each individual channel by the skew detectors (not shown), at step ~~102~~112. Since the deskew data for each channel is essentially a customized characterization of the channel (no averaging involved), optimizing the data, at step ~~104~~114, involves merely preserving the data. The deskew data is then stored, at step ~~106~~116, into a calibration table (memory) that cross-references the data to that particular channel.